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VS

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Salman Akram

Serial No.: 09/989,326

Filed: November 20, 2001

For: MULTIPLE DIE STACK APPARATUS EMPLOYING T-SHAPED INTERPOSER ELEMENTS

Examiner: Unknown

Group Art Unit: 2814

Attorney Docket No.: 2982.2US (96-712.2)

CERTIFICATE OF MAILING

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PRELIMINARY AMENDMENT

Box Non-Fee Amendment
Commissioner for Patents
Washington, D.C. 20231

Sir:

Prior to examination of the above-referenced patent application on the merits, entry of the amendments as set forth herein is respectfully solicited.

IN THE SPECIFICATION:

Please replace Paragraph **[0001]** as follows:

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[0001] This application is a continuation of application Serial No. 09/247,009, filed February 8, 1999, now U.S. Patent 6,351,028 B1, issued February 26, 2002.

IN THE CLAIMS:

Claims 1, 10-12, 15-17, 27-32, 36-41, 43, 49-53, 62-64, 67-71 and 79-82 have been amended herein. All of the pending claims 1 through 82 are presented, pursuant to 37 C.F.R. §§ 1.121(c)(1)(i) and 1.121(c)(3), in clean form below. Please enter these claims as amended. Attached is a marked-up version of the claims amended herein pursuant to 37 C.F.R. § 1.121(c)(1)(ii).

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1. (Amended) An interposer apparatus for use between a first semiconductor device and a second semiconductor device, said first semiconductor device and said second semiconductor device each having a plurality of bond pads disposed on an active surface thereof and a bottom surface, comprising:

a first surface having a first length and a first width;

a second surface having a length and a width smaller than said first width of said first surface, said first surface comprising an overhang portion of said apparatus for protection of said plurality of bond pads disposed on said first semiconductor device and said second surface being mountable to said active surface of said first semiconductor device.

2. The interposer apparatus according to claim 1, wherein said overhang portion further comprises at least one conductive strip for connection to at least one bond pad of said plurality of bond pads of said first semiconductor device.

3. The interposer apparatus according to claim 1, wherein said first and second surfaces are formed from a common unitary member.

4. The interposer apparatus according to claim 1, wherein said apparatus provides thermal conductivity for thermal energy transfer from said first semiconductor device and said second semiconductor device, each mounted to said apparatus.

5. The interposer apparatus according to claim 1, wherein said apparatus provides thermal insulation between said first semiconductor device and said second semiconductor device, each mounted to said apparatus.

6. The interposer apparatus according to claim 1, wherein said apparatus provides one of thermal conductivity and thermal insulation between said first semiconductor device and said second semiconductor device, each mounted to said apparatus.

7. The interposer apparatus according to claim 1, wherein said apparatus provides electrical insulation between said first semiconductor device and said second semiconductor device, each mounted to said apparatus.

8. The interposer apparatus according to claim 1, wherein said apparatus provides thermal insulation and electrical insulation between said first semiconductor device and said second semiconductor device, each mounted to said apparatus.

9. The interposer apparatus according to claim 1, wherein said apparatus provides thermal conductivity and electrical insulation between said first semiconductor device and said second semiconductor device, each mounted to said apparatus.

10. (Amended) The interposer apparatus according to claim 3, wherein said common unitary member has a coefficient of thermal expansion substantially equal to that of said first semiconductor device.

11. (Amended) The interposer apparatus according to claim 3, wherein said common unitary member has a coefficient of thermal expansion substantially equal to that of said second semiconductor device.

12. (Amended) The interposer apparatus according to claim 3, wherein said common unitary member has a coefficient of thermal expansion substantially equal to that of said first semiconductor device and said second semiconductor device.

13. The interposer apparatus according to claim 1, wherein said first surface of said apparatus is connected to a base portion of said second semiconductor device.

14. The interposer apparatus according to claim 1, wherein a third semiconductor device is mounted adjacent said second semiconductor device.

15. (Amended) The interposer apparatus according to claim 1, wherein said length of said second surface is substantially the same as said first length of said first surface.

16. (Amended) The interposer apparatus according to claim 1, wherein said length of said second surface is substantially the same as the width of said second surface.

17. (Amended) An interposer apparatus for use between a first semiconductor device and a second semiconductor device, said first semiconductor device and said second semiconductor device each having a plurality of bond pads on an active surface thereof and a bottom surface, said apparatus comprising:

a first surface having a first length and a first width;

a second surface having a length and a width smaller than said first width of said first surface, said first surface comprising an overhang portion of said apparatus for protection of said plurality of bond pads disposed on said first semiconductor device and said second surface being mountable to said active surface of said first semiconductor device;

a third surface having a first length and a first width; and

a fourth surface having a length and a width smaller than said first width of said third surface, said third surface providing an overhang portion of said apparatus for protection of said

plurality of bond pads disposed on said second semiconductor device and said fourth surface being mountable to said active surface of said second semiconductor device.

18. The interposer apparatus according to claim 17, wherein said overhang portion further comprises at least one conductive strip for connection to at least one bond pad of said plurality of bond pads of said first semiconductor device.

19. The interposer apparatus according to claim 17, wherein said first and second surfaces are formed from a common unitary member.

20. The interposer apparatus according to claim 17, wherein said third and fourth surfaces are formed from a common unitary member.

21. The interposer apparatus according to claim 17, wherein said apparatus provides thermal conductivity for thermal energy transfer from said first semiconductor device and said second semiconductor device, each mounted to said apparatus.

22. The interposer apparatus according to claim 17, wherein said apparatus provides thermal insulation between said first semiconductor device and said second semiconductor device, each mounted to said apparatus.

23. The interposer apparatus according to claim 17, wherein said apparatus provides one of thermal conductivity and thermal insulation between said first semiconductor device and said second semiconductor device, each mounted to said apparatus.

24. The interposer apparatus according to claim 17, wherein said apparatus provides electrical insulation between said first semiconductor device and said second semiconductor device, each mounted to said apparatus.

25. The interposer apparatus according to claim 17, wherein said apparatus provides thermal insulation and electrical insulation between said first semiconductor device and said second semiconductor device, each mounted to said apparatus.

26. The interposer apparatus according to claim 17, wherein said apparatus provides thermal conductivity and electrical insulation between said first semiconductor device and said second semiconductor device mounted to said apparatus.

27. (Amended) The interposer apparatus according to claim 19, wherein said common unitary member has a coefficient of thermal expansion substantially equal to that of said first semiconductor device.

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28. (Amended) The interposer apparatus according to claim 20, wherein said common unitary member has a coefficient of thermal expansion substantially equal to that of said first semiconductor device.

29. (Amended) The interposer apparatus according to claim 19, wherein said common unitary member has a coefficient of thermal expansion substantially equal to that of said second semiconductor device.

30. (Amended) The interposer apparatus according to claim 20, wherein said common unitary member has a coefficient of thermal expansion substantially equal to that of said second semiconductor device.

31. (Amended) The interposer apparatus according to claim 19, wherein said common unitary member has a coefficient of thermal expansion substantially equal to that of said first semiconductor device and said second semiconductor device.

32. (Amended) The interposer apparatus according to claim 20, wherein said common unitary member has a coefficient of thermal expansion substantially equal to that of said first semiconductor device and said second semiconductor device.

33. The interposer apparatus according to claim 17, wherein said first surface of said apparatus is connected to a base portion of said second semiconductor device.

34. The interposer apparatus according to claim 17, wherein said third surface of said apparatus is connected to a base portion of a third semiconductor device.

35. The interposer apparatus according to claim 17, wherein a third semiconductor device is mounted adjacent said second semiconductor device.

36. (Amended) The interposer apparatus according to claim 17, wherein said length of said second surface is substantially the same as said first length of said first surface.

37. (Amended) The interposer apparatus according to claim 17, wherein said length of said second surface is substantially the same as the width of said second surface.

38. (Amended) The interposer apparatus according to claim 17, wherein said length of said fourth surface is substantially the same as said first length of said third surface.

39. (Amended) The interposer apparatus according to claim 17, wherein said length of said fourth surface is substantially the same as the width of said fourth surface.

40. (Amended) An interposer apparatus for use between a plurality of semiconductor devices, each semiconductor device of said plurality of semiconductor devices having at least one bond pad on an active surface thereof and a bottom surface, comprising:

a first surface having a first length and a first width;

a second surface having a length and a width smaller than said first width of said first surface, said first surface providing a protective overhang portion that protects the at least one bond pad on an active surface of a first semiconductor device and said second surface being mountable to said active surface of said first semiconductor device.

41. (Amended) The interposer apparatus according to claim 40, wherein said protective overhang portion further comprises at least one conductive strip for connecting to said first semiconductor device.

42. The interposer apparatus according to claim 40, wherein said first and second surfaces are formed from a unitary member.

43. (Amended) The interposer apparatus according to claim 40, further comprising:

a third surface having a first length and a first width; and

a fourth surface having a length and a width smaller than said first width of said third surface, said third surface providing a portion that is at least partially covering said at least one bond pad on an active surface of a second semiconductor device and said fourth surface being mountable to said active surface of said second semiconductor device.

44. The interposer apparatus according to claim 40, wherein said apparatus provides thermal and electrical insulation between said first semiconductor device and a second semiconductor device of said plurality of semiconductor devices connected to said apparatus.

45. The interposer apparatus according to claim 40, wherein said apparatus provides thermal conductivity and electrical insulation between said first semiconductor device and a second semiconductor device of said plurality of semiconductor devices connected to said apparatus.

46. The interposer apparatus according to claim 42, wherein said unitary member has a coefficient of thermal expansion substantially the same as said first semiconductor device.

47. The interposer apparatus according to claim 40, wherein said first surface of said apparatus is connected to a base portion of a second semiconductor device of said plurality of semiconductor devices.

48. The interposer apparatus according to claim 47, wherein at least a third semiconductor device mounts adjacent said second semiconductor device of said plurality of semiconductor devices.

49. (Amended) The interposer apparatus according to claim 40, wherein said length of said second surface is substantially the same as said first length of said first surface.

50. (Amended) The interposer apparatus according to claim 40, wherein said length of said second surfaces is substantially the same as the width of said second surface.

51. (Amended) A stack of semiconductor devices on a substrate comprising:

a first semiconductor device having at least one bond pad on an active surface thereof, mounted to said substrate;

a first interposer device mounted to said first semiconductor device, on a side opposite said substrate, said first interposer device having a first surface of a first area and a second surface of a second area less than said first area with a first pair of recesses formed on opposing edges of said first interposer device exposing said at least one bond pad on said active surface of said first semiconductor device, said second surface mounted to said active surface of said first semiconductor device; and

a second semiconductor device, mounted to said first surface of said first interposer device, opposite said first semiconductor device.

52. (Amended) The stack according to claim 51, further comprising:

a second interposer device having a first side and a second side, said second interposer device being mounted to said second semiconductor device on said first side thereof, wherein said second interposer device includes a bond pad recess opening for allowing connection between said first and second semiconductor devices, or between said semiconductor devices and said substrate, or both.

53. (Amended) A conductive apparatus interposed between a first semiconductor device and a second semiconductor device, said first semiconductor device and said second semiconductor device each having a plurality of bond pads on an active surface thereof and a bottom surface, said apparatus comprising:

a first surface having a first length and a first width;

a second surface having a length and a width smaller than said first width of said first surface, said first surface comprising an overhang portion of said apparatus that protects said plurality of bond pads disposed on said first semiconductor device and said second surface being mountable to said active surface of said first semiconductor device.

54. The apparatus according to claim 53, wherein said overhang portion further comprises at least one conductive strip for connection to at least one bond pad of said plurality of bond pads of said first semiconductor device.

55. The apparatus according to claim 53, wherein said first and second surfaces are formed from a common unitary member.

56. The apparatus according to claim 53, wherein said apparatus provides thermal conductivity for thermal energy transfer from said first semiconductor device and said second semiconductor device, each mounted to said apparatus.

57. The apparatus according to claim 53, wherein said apparatus provides electrical insulation between said first semiconductor device and said second semiconductor device, each mounted to said apparatus.

58. The apparatus according to claim 53, wherein said apparatus provides one of thermal conductivity and thermal insulation between said first semiconductor device and said second semiconductor device, each mounted to said apparatus.

59. The apparatus according to claim 53, wherein said apparatus provides electrical insulation between said first semiconductor device and said second semiconductor device, each mounted to said apparatus.

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60. The apparatus according to claim 53, wherein said apparatus provides thermal conductivity and electrical insulation between said first semiconductor device and said second semiconductor device, each mounted to said apparatus.

61. The apparatus according to claim 53, wherein said apparatus provides thermal insulation and electrical insulation between said first semiconductor device and said second semiconductor device, each mounted to said apparatus.

62. (Amended) The apparatus according to claim 55, wherein said common unitary member has a coefficient of thermal expansion substantially equal to that of said first semiconductor device.

63. (Amended) The apparatus according to claim 55, wherein said common unitary member has a coefficient of thermal expansion substantially equal to that of said second semiconductor device.

64. (Amended) The apparatus according to claim 55, wherein said common unitary member has a coefficient of thermal expansion substantially equal to that of said first semiconductor device and said second semiconductor device.

65. The apparatus according to claim 53, wherein said first surface of said apparatus is connected to a base portion of said second semiconductor device.

66. The apparatus according to claim 65, wherein a third semiconductor device is mounted adjacent said second semiconductor device.

67. (Amended) The apparatus according to claim 53, wherein said length of said second surface is substantially the same as said first length of said first surface.

68. (Amended) The apparatus according to claim 53, wherein said length of said second surface is substantially the same as the width of said second surface.

69. (Amended) A conductive apparatus for interposing between a plurality of semiconductor devices, each semiconductor device of said plurality of semiconductor devices having at least one bond pad on an active surface thereof and a bottom surface, comprising:
a first surface having a first length and a first width;
a second surface having a length and a width smaller than said first width of said first surface, said first surface providing a protective overhang portion over said at least one bond pad on an active surface of a first semiconductor device of said plurality of semiconductor devices and said second surface being mountable to said active surface of said first semiconductor device.

70. (Amended) The apparatus according to claim 69, further comprising:

a third surface having a first length and a first width;

a fourth surface having a length and a width smaller than said first width of said third surface, said third surface providing a protective overhang portion that protects said at least one bond pad on an active surface of a second semiconductor device of said plurality of semiconductor devices and said fourth surface being mountable to said active surface of said second semiconductor device.

71. (Amended) The apparatus according to claim 69, wherein said protective overhang portion further comprises at least one conductive strip for connecting to said first semiconductor device.

72. The apparatus according to claim 69, wherein said first and second surfaces are formed from a unitary member.

73. The apparatus according to claim 70, wherein said third and fourth surfaces are formed from a unitary member.

74. The apparatus according to claim 69, wherein said apparatus provides thermal conductivity, thermal insulation, and electrical insulation between said first semiconductor device and a second semiconductor device of said plurality of semiconductor devices connected to said apparatus.

75. The apparatus according to claim 72, wherein said unitary member has a coefficient of thermal expansion substantially the same as said first semiconductor device.

76. The apparatus according to claim 73, wherein said unitary member has a coefficient of thermal expansion substantially the same as said first semiconductor device.

77. The apparatus according to claim 69, wherein said first surface of said apparatus is connected to a base portion of a second semiconductor device of said plurality of semiconductor devices.

78. The apparatus according to claim 77, wherein at least a third semiconductor device mounts adjacent said second semiconductor device of said plurality of semiconductor devices.

79. (Amended) The apparatus according to claim 69, wherein said length of said second surface is substantially the same as said first length of said first surface.

80. (Amended) The apparatus according to claim 69, wherein said length of said second surfaces is substantially the same as the width of said second surfaces.

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81. (Amended) A stack of semiconductor devices on a substrate comprising:

a first semiconductor device having at least one bond pad on an active surface thereof, mounted to said substrate;

a thermally conductive first interposer device mounted to said first semiconductor device, on a side opposite said substrate, said first interposer device having a first surface of a first area and a second surface of a second area less than said first area with a first pair of recesses formed on opposing edges of said first interposer device exposing said at least one bond pad on said active surface of said first semiconductor device, said second surface mounted to said active surface of said first semiconductor device; and

a second semiconductor device, mounted to said first surface of said first interposer device, opposite said first semiconductor device.

82. (Amended) The stack according to claim 81, further comprising:

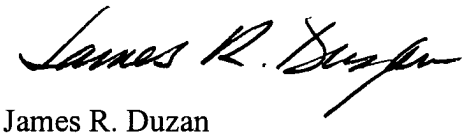
a second thermally conductive interposer device having a first side and a second side, said second thermally conductive interposer device being mounted to said second semiconductor

device on said first side thereof, wherein said second thermally conductive interposer device includes a bond pad recess opening for allowing connection between said first and second semiconductor devices, or between said semiconductor devices and said substrate, or both.

REMARKS

No new matter has been added. The Applicant again requests entry of the amendments as set forth in the Appendices hereto prior to examination of the application on the merits.

Respectfully submitted,



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Date: March 12, 2002
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